REMARKS

This is in furtherance to the Notice of Appeal mailed on January 22, 2008 which was in response to the final Office Action mailed August 21, 2007. Attached are an Electronic Fee Transmittal and the requisite extension fee for a one-month extension of time, to April 22, 2008. Claim 3 has been previously canceled without prejudice. Claims 1 and 15 have been amended. No new matter has been added to the application. No fee for additional claims is due by way of this Amendment. The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090. Claims 1-2 and 4-20 are pending.

A Request for Continued Examination (RCE) is filed concurrently with this Amendment to remove the application from the appeal process, so that the Office Action mailed August 21, 2007 is effectively made non-final. Under 37 U.S.C. 1.114, the effect of the RCE, which makes the instant Office Action non-final, is to cause examination of the instant application to remain open. Accordingly, arguments submitted herein are to be entered as a matter of right, and each claim is entitled to continued examination, particularly with respect to the responses provided herein.

Rejections Under 35 U.S.C. § 103

I. Claims 1-7 and 13-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over O'Connell et al. U.S. Patent No. 6,006,340 (hereinafter "O'Connell") in view of Holm et al. U.S. Patent No. 6,687,225 (hereinafter "Holm").

Claim 1 recites, *inter alia*, "the read control logic in the storage buffer control circuit is adapted to control the read pointer register such that data in the storage locations is only read after a predetermined time delay, the time delay being such that when all the said storage locations are read from successively a complete data packet without gaps is applied to the data output of the storage buffer circuit." (Emphasis added.)

The combination of O'Connell and Holm does not teach or suggest the invention of claim 1. As admitted in the Office Action, O'Connell does not disclose that the storage locations are not read until a predetermined time delay. Thus, O'Connell does not teach or

suggest that "data in the storage locations is only read after a predetermined time delay," as recited in claim 1.

Holm fails to cure the deficiencies of O'Connell. In particular, Holm does not teach or suggest a read control logic to control a read pointer register such that data in storage locations are only read after a predetermined time delay nor having a complete data packet without gaps. Instead, Holm teaches a fixed speed data interface controller configured to start extracting data from a FIFO only after a set amount of data is in the FIFO. *See. e.g.*, col. 2, lines 4-6. "If the FIFO runs out of data before the entire data packet or frame has been transmitted, a FIFO under run occurs which corrupts the transmission." *See, e.g.* col. 2, lines 14-17. To prevent such an occurrence, the required amount of data to be stored in the FIFO prior to extracting is calculated so as to accommodate the worst-case data routing circuit delays. *See e.g.*, col. 2, lines 17-20. Thus, Holm teaches that data is not extracted (i.e., read) until a set amount of data is stored while claim 1 recites that "data in the storage locations is only read after a predetermined time delay."

Furthermore, the amount of time necessary to fill the FIFO with the set amount of data is variable and is dependent upon the rate of data being sent to the FIFO in a particular situation. Such rate may change depending on the data throughput. It is clear that according to Holm, the threshold necessary to begin transferring data from the FIFO is not time dependent nor based on some time delay. Thus, there is no set amount of time which would guarantee that the minimum amount of data is stored in the FIFO prior to extraction. Consequently, Holm does not teach or suggest that "data in the storage locations is only read after a predetermined time delay," as recited in claim 1.

Thus, Holm does not cure the deficiencies of O'Connell.

Holm also teaches away from the invention of claim 1. Holm teaches that difficulties occur when the amount of data stored in the FIFO is not large enough to trigger a start threshold. For example, Holm teaches that during a transmit operation, the data interface controller may not read a data frame from the FIFO if the last data frame transmitted by the data routing circuit is not large enough to trigger the start threshold. *See e.g.*, col. 2, lines 33-44. In order to ensure that smaller data frames are not left in the FIFO, Holm discloses a controller that

begins transmitting the data frames held in the FIFO if the amount of data stored in the FIFO is less than a minimum data threshold value and more than a selected amount of time had passed.

Holm therefore teaches that, in a system where data is read after a threshold has been reached, it is necessary to incorporate additional arrangements to account for individual frames that are not big enough to reach this threshold. This leads to obvious bus inefficiency given that there will be a period of time when the majority of the data packet has been read, but the end portion of the packet is waiting to be flushed. Therefore, the system of Holm will have gaps in the packet, while claim 1 recites "the time delay being such that when all the said storage locations are read from successively a complete data packet without gaps is applied to the data output of the storage buffer circuit."

Also, the time delay of Holm is used in an opposite manner to the time delay of claim 1. Holm does not disclose a predetermined time delay whose purpose is to delay the output of the data in the FIFO in order to allow the data to accumulate in the FIFO and be read back to back to improve bus efficiency. Instead, the time delay of Holm is for the purpose of removing the FIFO of data to prevent small data frames from becoming stuck in the FIFO, while the time delay of claim 1 is to delay the output of data such that data may accumulate and thereby improve bus efficiency. Consequently, Holm teaches away from claim 1.

According to the instant application, introducing a predetermined time delay in the current invention thus overcomes the inefficiency of waiting for the FIFO buffer to fill to a threshold before sending data. The advantage of waiting a predetermined number of clock cycles rather than waiting for a set amount of data to be written to the FIFO is that one can start sending data before the FIFO buffer is full and still read out a complete package, without gaps, in a faster clock domain. Once a read from the FIFO has been initiated, data may still continue to be written to the FIFO until it is full. This results in more efficient use of the BUS, since the time between a data word first entering the FIFO and being read from it is reduced, while maintaining complete packages at the output. With knowledge of the rate at which data is being sent into the FIFO it is possible to operate the bridging circuit with greater efficiency, since read out can begin at a time when following data will be written into the FIFO, which will fill up during the send operation and avoid wasted clock cycles.

These advantages are not found in the teaching of Holm. In particular, the only use of the time delay mentioned in Holm is to flush small portions of data from the FIFO, which is opposite of storing or accumulating data, as recited in claim 1. Hence, it is clear that the teachings of Holm would not motivate one of ordinary skill in the art to realize that a predetermined time delay by itself would improve bus efficiency in the manner of the current invention.

As discussed above, Holm only mentions waiting a predetermined time delay in conjunction with a system that fills to a minimum data threshold before sending.

The Examiner *must* take the references in their entirety, and cannot simply ignore portions that *teach away* from the claimed subject matter or otherwise argue against obviousness. *Bausch & Lomb v. Barnes-Hind/Hydrocurve, Inc.*, 230 U.S.P.Q. 416, 420 (Fed. Cir. 1986). It is impermissible to pick and choose from a reference only so much of it as will support a conclusion of obviousness to the exclusion of other parts necessary to a full appreciation of what the reference fairly suggests to one skilled in the art. *Id* at 419. The courts have long cautioned that consideration *must* be given "where the references diverge and *teach away* from the claimed invention." *Akzo N.V. v. International Trade Commission*, 1 U.S.P.Q.2d 1241, 1246 (Fed. Cir. 1986). In other words, the Examiner has not explained why one skilled in the art would ignore the clear and unambiguous teachings of Holm directed to a controller that begins transmitting the data frames held in the FIFO if the amount of data stored in the FIFO is less than a minimum data threshold value and more than a selected amount of time had passed. Instead, the Examiner has tried to fit this incompatible/inconsistent teaching of Holm with O'Connell to teach a read control logic in the storage buffer control circuit adapted to control the read pointer register such that data in the storage locations is only read after a predetermined time delay, as recited in claim 1.

Since Holm fails to cure the deficiencies of O'Connell and teaches away from the invention of claim 1, claim 1 is nonobvious in view of the combination of O'Connell and Holm. Thus, claim 1 is allowable as are claims 2-7 and 13-14, which depend therefrom.

It is respectfully noted that the Applicant has clearly noted a teaching missing from O'Connell, and in discussing Holm made clear that Holm does not supply the missing teaching. Thus, Applicant is clearly treating the references in combination.

II. Claims 8-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over O'Connell, in view of Holm, and in further view of Sadowski (U.S. 2005/007165).

O'Connell, Holm and Sadowski do not teach or suggest the invention of claim 8, which depends from claim 1. In particular, Sadowski fails to teach or suggest the features of claim 1 that are missing from O'Connell and Holm. More specifically, Sadowski does not teach or suggest the predetermined time delay of claim 1. The Office Action has cited Sadowski only for *purportedly* teaching a retiming circuit adapted to provide a plurality of possible degrees of retiming, including a mode signal input for receiving a mode signal indicating the currently required degree of retiming, the retiming circuit being responsive to the mode signal to provide the required degree of retiming. Thus, it seems unnecessary to further discuss the lack of the predetermined time delay in Sadowski. Consequently, claim 1 is nonobvious in view of O'Connell, Holm and Sadowski as are claims 8-11, which depend therefrom.

It is respectfully noted that the Applicant has clearly noted a teaching missing from O'Connell and Holm, and in discussing Sadowski made clear that Sadowski does not supply the missing teaching. Thus, Applicant is clearly treating the references in combination.

Additionally, it is respectfully submitted that Sadowski does not teach or suggest the limitations recited in claim 8. In particular, Sadowski does not teach or suggest a retiming circuit "adapted to provide a plurality of possible degrees of retiming, and including a mode signal input for receiving a mode signal indicating the currently required degree of retiming, the retiming circuit being responsive to the mode signal to provide the required degree of retiming," as recited in claim 8.

Instead, Sadowski discloses a system for determining a processing speed of an integrated circuit. A multiplexer 132 receives a select delay signal indicating which one of the delays is to be chosen as an output signal. *See e.g.*, Figure 1 and paragraph [0018]. The multiplexer 132 selects a delay signal from a plurality of clock-adjusting circuits 124, 126, 128, 130 which are similar to the delay circuit 120 *See e.g.*, Figure 1 and paragraph [0017]. The clock-adjusting circuits 124, 126, 128, 130 generate possible degrees of delay, but do not teach possible degrees of retiming a signal into a specific clock domain. The clock-adjusting circuits

124, 126, 128, 130 of Sadowski are not clocked and therefore cannot retime a signal to a clock source. Thus, Sadowski does not teach or suggest the limitations recited in claim 8.

Since Sadowski fails to cure the deficiencies of O'Connell and Holm and also does not even teach or suggest the limitations recited in claim 8, claims 8 is nonobvious in light of the combined teachings of O'Connell, Holm and Sadowski. Thus, claim 8 is allowable as are claims 9-11, which depend therefrom.

III. Claim 12 was rejected under 35 U.S.C. § 103(a) as being unpatentable over O'Connell, in view of Holm, and in further view of Cavanna et al. (U.S. 6,208,703).

O'Connell and Holm do not teach or suggest the invention of claim 12 which depends on claim 1. In particular, Cavanna fails to teach or suggest the features of claim 1 that are missing from O'Connell and Holm. More specifically, Cavanna does not teach or suggest that data is not read until a predetermined time delay. Instead, Cavanna teaches that "the not empty output indicates whether stored data may be read." *See e.g.*, col. 1, lines 60-61. Thus, Cavanna does not cure the deficiencies of O'Connell and Holm.

Consequently, claim 1 is nonobvious in view of O'Connell, Holm and Cavanna as is claim 12, which depends therefrom.

It is respectfully noted that the Applicant has clearly noted a teaching missing from O'Connell and Holm, and in discussing Cavanna made clear that Cavanna does not supply the missing teaching. Thus, Applicant is clearly treating the references in combination.

IV. Claims 15-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over O'Connell, in view of Holm, and in further view of Sadowski.

It is respectfully noted that the Office Action sets forth arguments contending that the teachings of O'Connell and Sadowski are anticipatory of the limitations of claims 15-20. The Office Action makes no reference whatsoever to Holm in any of the arguments pertaining to claims 15-20. However, in the interest of furthering prosecution of the case, applicants first submit arguments to traverse the combination of O'Connell, Holm, and Sadowski and then address the specific arguments set forth in the Office Action.

Claim 15 recites, *inter alia*, "a selector connected to receive inputs from each of the retiming buffers…the storage buffer output clock rate comprising one or more retiming buffers and a selector connected to receive inputs from each of the retiming buffers…wherein the storage buffer control circuit is adapted to control the selectors such that zero or more retiming buffers are selectively in the path from the read or write pointer registers to the comparators and wherein, when one or more retiming buffers are in the path from the read or write pointer registers to the comparators, the read control logic is adapted to control the read pointer register such that data in the storage locations is only read after a predetermined time delay, the time delay being such that all the storage locations are read from successively and a complete data packet without gaps is provided to the data output." (Emphasis added.)

Although the language of claim 15 is not identical to that of claim 1, the allowablity of claim 15 over O'Connell and Holm is apparent in light of the above discussion.

Sadowski fails to cure the deficiencies of O'Connell and Holm. In particular, Sadowski fails to teach the features of claim 15 that are missing from O'Connell and Holm. Specifically, Sadowski does not teach "that data in the storage locations is only read after a predetermined time delay, the time delay being such that all the said storage locations are read from successively and a complete data packet without gaps is provided to the data output," as recited in claim 15. Instead, the Office Action has cited Sadowski only for *purportedly* teaching a system for determining a processing speed of an integrated circuit. Such is unrelated to the missing teachings of O'Connell and Holm.

As such, O'Connell, Holm and Sudowski fail to teach or suggest the invention of claim 15. Consequently, claim 15 is patentable over O'Connell, Holm and Sudowski as are claims 16-20 which depend therefrom.

It is respectfully noted that the Applicant has clearly noted a teaching missing from O'Connell and Holm, and in discussing Sadowski made clear that Sadowski does not supply the missing teaching. Thus, Applicant is clearly treating the references in combination.

Additionally, the Office Action asserts that O'Connell discloses all elements for of a bridge circuit for use in retiming a semiconductor integrated circuit recited in claim 15, except for a selector connected to receive inputs from each of the retiming buffers and a storage buffer control circuit that is adapted to control the selectors such that zero or more retiming

buffers are selectively in the path from the read or write pointer registers to the comparators. The Office Action contends that Sadowski contains this missing teaching. Such is respectfully traversed herein.

Sadowski fails to cure the deficiencies of O'Connell. Sadowski does not teach or suggest a selector connected to receive inputs from each of the retiming buffers and a storage buffer control circuit adapted to control the selectors such that zero or more retiming buffers are selectively in the path from the read or write pointer registers to the comparators. Instead, Sadowski discloses a system for determining a processing speed of an integrated circuit. A multiplexer 132 receives a select delay signal 142 indicating which one of the delays is to be chosen as an output signal. *See e.g.*, Figure 1 and paragraph [0018]. The multiplexer 132 selects a delay signal from a plurality of clock-adjusting circuits 124, 126, 128, 130 which are similar to the delay circuit 120 *See e.g.*, Figure 1 and paragraph [0017]. The clock-adjusting circuits 124, 126, 128, 130 generate possible degrees of delay, but do not teach possible degrees of retiming a signal into a specific clock domain. Even though the delay elements of Sadowski introduce a degree of delay into the circuit, the clock-adjusting circuits 124, 126, 128, 130 are not clocked and therefore cannot retime an input signal to a clock source. Thus, the clock-adjusting circuits 124, 126, 128, 130 are not retiming buffers.

Consequently, Sadowski does not teach or suggest "a selector connected to receive inputs from each of the retiming buffers" and that a "storage buffer control circuit is adapted to control the selectors such that zero or more retiming buffers are selectively in the path from the read or write pointer registers to the comparators," as recited in claim 15.

Since Sadowski fails to cure the deficiencies of O'Connell, claim 15 is nonobvious in view of O'Connell and Sadowski. Thus, claim 15 is allowable over O'Connell and Sadowski as are claims 16-20, which depend therefrom.

It is respectfully noted that the Applicant has clearly noted a teaching missing from O'Connell, and in discussing Sadowski made clear that Sadowski does not supply the missing teaching. Thus, Applicant is clearly treating the references in combination.

Conclusion

Overall, the cited references do not singly, or in any motivated combination, teach or suggest the claimed features of the embodiments recited in independent claims 1 and 15, and thus such claims are allowable. Because the remaining claims depend from the allowable independent claims, and also because they include additional limitations, such claims are likewise allowable. If the undersigned agent has overlooked a relevant teaching in any of the references, the Examiner is requested to point out specifically where such teaching may be found.

In light of the above amendments and remarks, Applicants respectfully submit that all pending claims are allowable. Applicants, therefore, respectfully request that the Examiner reconsider this application and timely allow all pending claims. Examiner is encouraged to contact Mr. Stern by telephone to discuss the above and any other distinctions between the claims and the applied references, if desired. If the Examiner notes any informalities in the claims, he is encouraged to contact Mr. Stern by telephone to expediently correct such informalities.

Respectfully submitted,

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